I Claim:

1. A circuit configuration for regenerating clock signals, comprising:

an input differential amplifier generating first and second amplified signals in response to first and second differential input clock signals;

first and second inverters connected to said input differential amplifier and generating respective first and second differential output clock signals; and

an offset compensation circuit connected to said first and said second inverters and adjusting a difference between the two output clock signals to a constant value.

2. The circuit configuration according to claim 1, wherein said first and said second inverters generate the first and the second differential output clock signals from the first and second amplified signals.

3. The circuit configuration according to claim 1, wherein the constant value is zero.

4. The circuit configuration according to claim 1, wherein said offset compensation circuit has:

a control amplifier having an input receiving the two output clock signals and outputting output signals derived from the output clock signals, and

a further differential amplifier generating first and second amplified, offset-compensated signals from the first and second amplified signals of said input differential amplifier and the output signals of said first control amplifier and feeding the first and second amplified, offset-compensated signals as drive signals to said inverters.

5. The circuit configuration according to claim 4, wherein said further differential amplifier feeds the first and second amplified, offset-compensated signals directly to said inverters.

6. The circuit configuration according to claim 4, wherein said further differential amplifier feeds the first and second amplified, offset-compensated signals to said inverters via a further component.

7. The circuit configuration according to claim 6, wherein said further component is a further differential amplifier.

8. The circuit configuration according to claim 4, further comprising an additional control circuit for driving said two

inverters to shift input pulse shapes of said inverters to an optimum switching point of said inverters.

9. The circuit configuration according to claim 8, wherein said control circuit for driving said two inverters has:

a further control amplifier having an input receiving an average value of the first and second differential output clock signals and a desired value, and

a third differential amplifier generating first and second drive signals for said first and second inverters in response to the first and second amplified offset-compensated signals of said differential amplifier and the output signal of said second control amplifier.

10. A circuit configuration for regenerating clock signals, comprising:

an input differential amplifier generating first and second amplified signals in response to first and second differential input clock signals;

first and second inverters connected to said input differential amplifier and generating respective first and second differential output clock signals from the first and

second amplified signals, said inverters having respective input pulse shapes and an optimum switching point; and

a control circuit for driving said inverters and shifting the input pulse shapes of said inverters to the optimum switching point of said inverters.

11. The circuit configuration according to claim 10, wherein said control circuit has:

a control amplifier having an input receiving an average value of the first and second differential output clock signals and a desired value and outputting an output signal, and

a differential amplifier generating first and second drive signals for said first and second inverters in response to the output signal of said control amplifier and input signals fed by one of said input differential amplifier and a component connected downstream thereof.

12. The circuit configuration according to claim 4, wherein said control amplifier is an integrator providing two input signals for said second differential amplifier for offset compensating the two differential output signals of said second differential amplifier.

13. The circuit configuration according to claim 12, wherein said integrator has an input; and

a high-frequency filter is connected upstream of said input of said integrator.

14. The circuit configuration according to claim 12, wherein, said second differential amplifier superposes an offset voltage on the two output signals by using a resistor and two currents controlled by said first integrator.

15. The circuit configuration according to claim 9, wherein said further control amplifier is an integrator.

16. The circuit configuration according to claim 15, further comprising a voltage divider circuit providing an average value of the first and second differential output clock signals;

said integrator receiving an input signal representing the average value of the first and second differential output clock signals provided by said voltage divider circuit.

17. The circuit configuration according to claim 15, further comprising a voltage divider circuit providing an input signal to said integrator representing the desired value.

18. The circuit configuration according to claim 9, wherein:

said third differential amplifier has a current source, said current source providing a current to correct a duty cycle distortion of said first and second inverters by applying an offset voltage to drive signals for said first and second inverters; and

said output of said further control amplifier controls said current source of said third differential amplifier.

19. The circuit configuration according to claim 9, wherein:

said third differential amplifier controls two current sources providing respective currents; and

said current sources provide respective offset voltages, the respective offset voltages being applied to drive signals for said first and second inverters to correct a duty cycle distortion of said first and second inverters.

20. The circuit configuration according to claim 1, wherein the differential output clock signals are fed to a differential line driver.

21. The circuit configuration according to claim 1, wherein all of the circuit components are embodied using CMOS technology.